Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SEONG CHEOL SHIN

Appeal No. 2005-0343
Application No. 09/836,204[1]

HEARD: March 10, 2005

Before KRASS, BARRY and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-12. Claims 13-22 have been cancelled.

We reverse and enter a new rejection pursuant to 37 CFR § 41.50(b).

BACKGROUND

Appellant's invention relates to a technique for driving a plasma display panel utilizing an asymmetry sustaining such that

[1] Application for patent filed April 18, 2001, which claims the foreign filing priority benefit under 35 U.S.C. § 119 of Korean Application No. P00-20795, filed April 19, 2000.

the high sustaining voltage is allowed to stabilize in order to achieve high-speed driving. According to Appellant, the driving signal for the lower block is applied in such a manner to overlap with the upper driving signal (specification, page 9).

Representative independent claim 1 is reproduced as follows:

1. A method of driving a plasma display panel utilizing an asymmetry sustaining wherein the plasma display panel is divided into an upper block and a lower block for it's driving, said method comprising the steps of:

applying an upper driving signal for supplying a data to address electrode lines provided at the upper block; and

applying a lower driving signal for supplying a data to address electrode lines provided at the lower block in such a manner to overlap with the upper driving signal.

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Tokunaga et al. (Tokunaga)	5,995,069	Nov. 30, 1999
Kim et al. (Kim)	6,229,516	May 8, 2001 (filed Dec. 30, 1996)

Claims 1-12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tokunaga and Kim.

We make reference to the answer (Paper No. 15, mailed May 5, 2004) for the Examiner's reasoning, and to the brief (Paper No. 13, filed March 30, 2004) and the reply brief (Paper No. 16, filed July 6, 2004) for Appellant's arguments thereagainst.

OPINION

The Examiner relies on Tokunaga (Figures 9 and 11) for teaching a method for driving a plasma display by applying an upper driving signal and a lower driving signal to the upper and lower blocks, respectively (answer, page 3). The Examiner identifies asymmetry sustaining as being absent in the driving method of Tokunaga (id.). The Examiner, however, asserts that the missing limitation is disclosed by Kim as the asymmetry driving method for driving a flat panel display (id.), and reasons that providing such asymmetry driving method in Tokunaga to improve image quality would have been obvious since a plasma display is a flat panel display (id.).

Appellant argues that the asymmetrical driving method for a liquid crystal display by applying gate line signals at different times, as disclosed by Kim, is different from and may not be properly applied to a plasma display panel (brief, pages 7 & 8). Appellant asserts that although Kim mentions plasma display panels being used as computer monitors, there is no indication that a plasma display may be asymmetrically driven as stated by the Examiner (brief, page 9). Appellant further points out that it is not clear how the delay created in the lower and the upper data blocks due to the time difference of the start signals STV1

and STV2 may be implemented in a plasma display, which has a different driving technology than the LCD of Kim (reply brief, pages 3 & 4).

In response, the Examiner argues that a plasma display and an LCD are both dot matrix displays which require the same data (addressing) drivers and scanning drivers for applying data and scanning signals to the display panel (answer, page 5). The Examiner concludes that the disclosed asymmetry drive also applies to a plasma display since Kim uses an LCD merely as the representative display type for disclosing an asymmetry drive (id.).

As a general proposition, in rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) and In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). A prima facie case of obviousness is established when the teachings of the prior art itself would appear to have suggested the claimed subject matter to one of ordinary skill in the art. See In re Bell, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993); In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992); Uniroyal, Inc. v. Rudkin-Wiley

Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985). In considering the question of the obviousness of the claimed invention in view of the prior art relied upon, the Examiner is expected to make the factual determination set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. See also In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998).

A review of Tokunaga confirms that the reference relates to a driving system for a plasma display panel of a matrix display type (col. 1, lines 6-8). As depicted in Figure 11, a pair of pixel data electrode sets D1-D12 form an upper block and a lower block which are connected to their corresponding address drivers 34a and 34b (col. 9, lines 58-67). Kim, on the other hand, describes a display driving circuit for increasing the length of time the image signal is applied to the pixels (abstract). However, Kim discloses the details of applying scanning signals to the gate drivers and only in the context of an LCD.

We agree with Appellant (brief, page 8) that what the Examiner characterizes as asymmetry driving the flat panel display in Figures 2 and 9 of Kim is actually delayed gate signals STV1 and STV2 applied to the gate lines in the upper and the lower blocks of the matrix. Kim specifically discloses that the first start signal STV1 is applied to "the upper gate driver 22 to start applying scanning signal" whereas the second start signal STV2 is applied to "the lower gate driver 24 to begin to apply scanning signal" (col. 8, lines 13-20). As depicted in Figure 2, although Kim shows two separate data (address) drivers 12 and 14 for the upper and the lower blocks, there is nothing in the reference to indicate how they are driven other than simultaneously. We also agree with Appellant (oral hearing) that the delayed gate signals are actually applied to the row electrodes and not to the address electrode lines.

Based on our findings above, we disagree with the Examiner that Tokunaga and Kim may be properly combined to suggest delaying the signal supplied to the address electrode line at the upper block with respect to that of the lower block. Accordingly, as the Examiner has failed to provide sufficient evidence to support a prima facie case of obviousness, the 35 § 103 of claims 1-12 cannot be sustained.

CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1-12 under 35 U.S.C. § 103 is reversed.

We make the following new ground of rejection for claims 1 and 7 under 35 U.S.C. § 102 as being anticipated by Appellant's admitted prior art, as depicted in Figures 2 and 4, pursuant to 37 CFR § 41.50(b).

Claims 1 and 7 are rejected under 35 U.S.C. § 102(e)(2) as being anticipated by the admitted prior art.

Initially, we note that claim 1 recites "an asymmetry sustaining" only in the preamble of the claim without any specific link to the recited features in the body of the claim that provide an asymmetry sustaining. In that regard, when broadly interpreted, the limitation of "in such a manner to overlap with the upper driving signal" is neither dependent on the preamble for its antecedent basis nor defined by it. Where a patentee uses the claim preamble to recite structural limitations of his claimed invention, the PTO and courts give effect to that usage. Bell Communications Research, Inc. v. Vitalink Communications Corp., 55 F.3d 615, 620, 34 USPQ2d 1816, 1820 (Fed. Cir. 1995). See also Corning Glass Works v. Sumitomo Elec. U.S.A., Inc., 868 F.2d 1251, 1257, 9 USPQ2d 1962, 1966 (Fed. Cir.

1989). Conversely, where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention, the preamble is not a claim limitation. See Bell Communications, 55 F.3d at 620; Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Therefore, contrary to Appellant's assertion that this claim limitation necessarily means "partial overlap" (oral hearing), claim 1 merely requires that the two signals "overlap" without specifying the extent of the overlap or the portion in common. The admitted prior art in Figure 4 shows that signal "X TOP" applied to address electrode lines in the upper block overlaps with the upper driving signal, "X BOTTOM." Additionally, the admitted prior art shows that the energy recovery circuit is driven ("X E/R UP" and "X E/R DN") such that the address driving signals are raised into a stable voltage level and then allowed to fall into a ground voltage level, as recited in claim 7.

In view of the discussion above, Appellant's admitted prior art anticipates claims 1 and 7 as all the claimed elements are disclosed. Accordingly, we find that claims 1 and 7 are unpatentable under 35 U.S.C. § 102.

In addition to reversing the Examiner's decision with respect to the 35 U.S.C. § 103, this decision contains a new ground of rejection pursuant to 37 CFR § 41.50(b) (effective September 13, 2004, 69 Fed. Reg. 49960 (August 12, 2004), 1286 Off. Gaz. Pat. Office 21 (September 7, 2004)). 37 CFR § 41.50(b) provides "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 CFR § 41.50(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

(1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .

(2) Request rehearing. Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .37 CFR § 1.196(b) provides that "[a] new ground of rejection shall not be considered final for purposes of judicial review."

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

REVERSED
37 CFR § 41.50(b)

ERROL A. KRASS
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

MAHSHID D. SAADAT
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

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